Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**GATE**

**BASE**

**DRAIN**

**23 mils**

**23 mils**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 4391**

**APPROVED BY: DK DIE SIZE .023” X .023” DATE: 11/24/20**

**MFG: LINEAR SYSTEMS THICKNESS .006” P/N: J309**

**DG 10.1.2**

#### Rev B, 7/19/02